UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,933	10/17/2001	Satoshi Inaba	P 284023 TRN-98S1152-D	4031

909 7590 03/31/2003

PILLSBURY WINTHROP, LLP
P.O. BOX 10500
MCLEAN, VA 22102

EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/977,933	Applicant(s) INABA, SATOSHI	
	Examiner Michael Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/235,310* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3 & 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's election filed on January 16, 2003. Claims 15-20 are elected. Non elected claims 1-14,21-34 were canceled by Applicant.

Claim Rejections - 35 USC § 112

1. Claims 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 15 (page 47, line 15): meaning and scope of "subjected to the steps" are unclear and indefinite for which steps.

(Dependent claims are also rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Isao (JP-04-093080).

Isao teaches a method for forming a semiconductor device comprising at least the steps of: forming an etching mask of a first insulating film 9,10 having an opening portion (Figs 2b,4a,4b); forming a trench 200 in the semiconductor substrate 100 by etching (Fig 4b,1b; English Abstract); forming a gate insulating film 11 of a second insulating film on an inner surface of the trench 200; forming a gate material film 12 on the second insulating film 11 (Fig 4b); patterning the gate film to form a gate (12A' in Fig 4c and 12B in Fig 4f) on a central portion of the trench and on source/drain side; implanting impurity ions to form source and drain

extension regions 23 (Fig 4c); forming a third insulating film to cover the semiconductor substrate and forming gate sidewall spacers 29 of a third insulating film (Fig 4g) by anisotropically etching to cover the inner surface of the trench extending on the source/drain side of the gate 12B; and implanting ions into the source and drain regions using the gate 12B having the spacers 29 as a mask to form a MIS transistor having source and drain regions 32,32' being close to or adjacent to side surfaces of the trench and connected the source and drain extension regions 23,23' on the bottom surface of the trench. Re claim 16, wherein the trench 200 is isotropically etched so that side surfaces of the trench 200 having a rounded surface (fig 1b,4b).

4. Claims 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn et al (5,342,796).

Ahn teaches a method for forming MIS semiconductor device at least comprising: forming an etching mask of a first insulating film 3 having an opening (Figs 3-4); forming a shallow trench having a plat bottom surface in at least a semiconductor substrate in corresponding with the (Fig 5, figs 7-9; col 4, lines 5-60); forming a gate insulating film of a second insulating film 7 and forming a gate material film 8 (Fig 6); patterning the gate film to form a gate 9 on a central portion of the trench and on source/drain side; implanting impurity ions to form source and drain extension regions 11 (Fig 8); forming a third insulating film to cover the semiconductor substrate and forming gate sidewall spacers 12 of a third insulating film by anisotropically etching to cover the inner surface of the trench extending on the source/drain side of the gate 9; and implanting ions into the source and drain regions using the gate having the spacers 12 as a mask to form a MIS transistor having source and drain regions 13 being close to or adjacent to side surfaces of the trench and connected the source and drain extension regions 11 on the bottom surface of the trench. Re claim 16, wherein the trench is etched wet etchant which is inherently etched in isotropic direction so that side surfaces of the trench are constituted a rounded surface (col 3, lines 13-21).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isao (JP04-093080) or Ahn et al (5,342,796) taken with Jeuch et al (4,939,100) and Lee et al (5,583,064).

Isao or Ahn teaches a MIS semiconductor device as applied above to claims 15-16.

Isao or Ahn lacks implanting ions into the bottom surface only to control a threshold voltage.

However, *Jeuch et al* teach (at fig 5F-5I; col 7, lines 10-21) to implant impurity ions into the bottom surface of the concave only, and thus inherently control a threshold voltage of the MIS semiconductor device. *Lee et al* teach to control a threshold voltage by implanting impurity ions only into the bottom surface of the concave (figs 5B,5C, 5H; col 5, lines 15-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Isao or Ahn by including impurity ions only at the bottom surface of the concave as taught by Jeuch and Lee. This is because of the desirability to control threshold voltage of the MIS semiconductor device.

7. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isao (JP04-093080) taken with Bronner et al (5,362,663).

Isao teaches a semiconductor device method as applied above to claims 15-16.

Isao does not mention the first insulating film of TEOS oxide, the second insulating film of thermal oxide, and the third insulating film of SiN for spacers, and the buffer layer of thermal oxide (claims 18-19).

However, Bronner et al teach the first insulating film 52 of TEOS oxide (col 6, lines 12-16; Fig 3), the second insulating film 60 of thermal oxide (col 8, lines 5-10), and the third insulating film of SiN for spacers 72 (col 8, lines 28-30; Fig 9), and the buffer layer 50 of thermal oxide (col 6, lines 10-15,28-35; Fig 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Isao by forming the first insulating film

of TEOS oxide, the second insulating film of thermal oxide, and the third insulating film of SiN for spacers, and the buffer layer of thermal oxide, as taught by Bronner et al, because these materials have proven in the art to be effectively and alternatively used as an insulating materials and as masking materials for protecting the underlying layers during subsequent etching and ion implantation.

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isao (JP04-093080) or Ahn et al (5,342,796) taken with Rodder et al (5,079,180).

Isao or Ahn teaches a semiconductor device method as applied above to claims 15-16.

Isao or Ahn lacks heating a high melting point metal to form silicide on source/drain regions and polysilicon gate.

However, Rodder et al teach (at Fig 2C-2D; col 5, lines 20-34) to reduce contact resistance by forming a high melting point metal layer to cover the substrate; heating the high melting point metal to form silicide 72,74 on source/drain regions and polysilicon gate; and removing the high melting point metal remaining on the spacers.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Isao or Ahn by employing the process of forming a high melting point metal layer to cover the substrate, heating the high melting point metal to form silicide on source/drain regions and polysilicon gate, and removing the high melting point metal remaining on the spacers, as taught by Rodder et al. This is because of the desirability to reduce contact resistance.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner